AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claim 1. (currently amended): A MIS transistor, comprising:

a semiconductor substrate having a surface with a principal crystal plane comprising a projecting part formed directly from the surface of the semiconductor substrate and at least one of a top surface and a side wall of the projecting part has a secondary crystal plane different from the principal crystal plane ~~of which surfaces are at least two different crystal planes on a principal plane~~;

a gate insulator formed on the semiconductor substrate including the projecting part in such a way that the gate insulator covers at least a portion of the semiconductor substrate, the top surface and the side wall of the projecting part ~~for covering at least a part of each of said at least two different crystal planes constituting the surface of the projecting part~~;

a gate electrode formed on the gate insulator including the projecting part, said gate electrode being elongated in the direction of a gate length and in the direction of a gate width ~~comprised on said at least a part of each of said at least two different crystal planes constituting the surface of the projecting part so as to be electrically insulated therefrom by the gate insulator~~; and

a pair of diffusion regions ~~having the same conductivity type and~~ formed on both sides of the gate electrode in the direction of said gate length on the semiconductor substrate including the projecting part ~~in the projecting part so as to face said at least a part of each of said at least two different crystal planes constituting the surface of the projecting part~~.

Claim 2. (currently amended): The MIS transistor according to claim 1 wherein [[the]] a channel width of a channel of the MIS transistor formed along with the gate insulator is defined ~~between the pair of diffusion regions is indicated~~ by summation of each width of ~~each channel~~ channels formed ~~along each of said at least two different crystal planes~~ along with the gate insulator including the width and height of the projecting part.

Claim 3. (currently amended): The MIS transistor according to claim 1 wherein the gate insulator continuously covers the top surface and the side wall of the projecting part ~~said at least a part of each of said at least two different crystal planes, which configure the surface of the projecting part, so as to continuously cover said at least two different crystal planes~~.

Claim 4. (canceled).

Claim 5. (currently amended): The MIS transistor, comprising:

a semiconductor substrate having a surface with a principal crystal plane comprising a projecting part formed directly from the surface of the semiconductor substrate and at least one of a top surface and a side wall of the projecting part has a secondary crystal plane different from the principal crystal plane ~~of which surfaces have at least two different crystal planes on a principal plane~~;

a gate insulator covering at least a portion of the semiconductor substrate, the top surface and the side wall of the projecting part ~~each of said two different crystal planes of the surface of said projecting part, said gate insulator further covering at least a part of said principal plane of said substrate~~;

a gate electrode formed on [[said]] the gate insulator ~~so as to be~~ thereby the gate electrode is electrically insulated from the semiconductor substrate; and

a pair of diffusion regions of the same conductivity type formed on both sides of the gate electrode on the semiconductor substrate ~~at said two different crystal planes of said projecting part and at said principal plane of said substrate on both sides of said gate electrode~~.

Claim 6. (currently amended): The MIS transistor according to claim 5, wherein the gate insulator continuously covers the top surface and the side wall of the projecting part ~~at least each of said at least two different crystal planes and the principal plane so that the principal plane and said two different crystal planes are continuously covered~~.

Claims 7-8. (canceled).

Claim 9. (currently amended): The MIS transistor according to claim 1, ~~being~~ wherein the MIS transistor is a signal transistor.

Claim 10. (currently amended): The MIS transistor, according to claim 5, ~~being~~ wherein the MIS transistor is a signal transistor.

Claim 11. (previously presented): The MIS transistor according to claim 1, wherein the semiconductor substrate is a silicon substrate, and the gate insulator is formed by exposing the surface of the silicon substrate to a plasma of a prescribed inert gas so as to remove hydrogen, and the hydrogen content at an interface of the silicon substrate and the gate insulator is $10^{11}/cm^2$ or less in units of surface density.

Claim 12. (previously presented): The MIS transistor according to claim 5, wherein the semiconductor substrate is a silicon substrate, and the gate insulator is formed by exposing the surface of the silicon substrate to a plasma of a prescribed inert gas so as to remove hydrogen,

and the hydrogen content at an interface of the silicon substrate and the gate insulator is $10^{11}/cm^2$ or less in units of surface density.

Claim 13. (currently amended): The MIS transistor according to claim 11, wherein the semiconductor substrate is a silicon substrate, and each of the principal crystal plane and ~~said at least two different~~ the crystal planes of the top surface and the side wall of the projecting part are any two different crystal planes from the (100) plane, the (110) plane and the (111) plane.

Claim 14. (withdrawn): A CMOS transistor, comprising the MIS transistor according to claim 1, and also comprising an n-channel MOS transistor only formed on a principal plane of a semiconductor substrate and a p-channel MOS transistor, wherein the p-channel MOS transistor comprises that the gate insulator is an oxide film, and that the single conductivity type diffusion region is a p-type diffusion region.

Claim 15. (withdrawn): A CMOS transistor, comprising the MIS transistor according to claim 5, and also comprising an n-channel MOS transistor only formed on a principal plane of a semiconductor substrate and a p-channel MOS transistor, wherein the p-channel MOS transistor comprises that the gate insulator is an oxide film, and that the single conductivity type diffusion region is a p-type diffusion region.

Claim 16. (withdrawn): A CMOS transistor, comprising the MIS transistor according to claim 11, and also comprising an n-channel MOS transistor only formed on a principal plane of a semiconductor substrate and a p-channel MOS transistor, wherein the p-channel MOS transistor comprises that the gate insulator is an oxide film, and that the single conductivity type diffusion region is a p-type diffusion region.

Claim 17. (withdrawn): A CMOS transistor comprising the MIS transistor according to claim 1, and also comprising an n-channel MOS transistor and a p-channel MOS transistor on a silicon substrate with the (100) plane as its principal plane, wherein

the n-channel MOS transistor comprises

a gate oxide film covering a part of the principal plane alone,

a gate electrode configured on the principal plane by the gate oxide film so as to be electrically insulated from the silicon substrate, and

an n-type diffusion region formed in the silicon substrate facing the principal plane and formed on both sides of the gate electrode, and

the p-channel MOS transistor comprises

that the single conductivity type diffusion region is a p-type diffusion region;

that the gate insulator is an gate oxide film, and

that one crystal plane is the (100) crystal plane and a second crystal plane is the (110) crystal plane among said at least two crystal planes.

Claim 18. (withdrawn): A CMOS transistor comprising the MIS transistor according to claim 5, and also comprising an n-channel MOS transistor and a p-channel MOS transistor on a silicon substrate with the (100) plane as its principal plane, wherein

the n-channel MOS transistor comprises

a gate oxide film covering a part of the principal plane alone,

a gate electrode configured on the principal plane by the gate oxide film so as to be electrically insulated from the silicon substrate, and

an n-type diffusion region formed in the silicon substrate facing the principal plane and formed on both sides of the gate electrode, and

the p-channel MOS transistor comprises

that the single conductivity type diffusion region is a p-type diffusion region;

that the gate insulator is an gate oxide film, and

that one crystal plane is the (100) crystal plane and a second crystal plane is the (110) crystal plane among said at least two crystal planes.

Claim 19. (withdrawn): The CMOS transistor according to claim 16, wherein the current driving capacity in the p-channel MOS transistor and the n-channel MOS transistor are equal to each other and the element area of the p-channel MOS transistor and the n-channel MOS transistor are the same.